As illustrated in Figs. 1 and 2, a wafer stage chamber assembly 100 for use in manufacturing semiconductor substrates comprises a chamber frame 102 to enclose a wafer stage device 66 (shown in Fig. 8), and a plurality of chamber walls or panels 104, 106, 108, 110, attached to the chamber frame. Chamber frame 102 and chamber walls 104, 106, 108, and 110 construct a chamber portion 101. Wafer stage chamber assembly 100 also comprises a top wall 112 and a base frame 114 attached to the top and bottom sides 102A and 102B, respectively, of chamber frame 102. Chamber frame 102 has a first flange 148 surrounding an upper perimeter thereof. Similarly, top wall 112 has a second flange 122, corresponding and to interface with first flange 148, surrounding a perimeter of top wall 112. Detail of wafer stage chamber assembly 100 is disclosed in U.S. Patent Application Serial No. 09/759,218, filed January 16, 2001, the entire disclosure of which is incorporated by reference.

IN THE CLAIMS:

Please amend claims 15, 19, and 23, as follows:

15. (Amended) A chamber seal device that seals a chamber assembly, the chamber assembly having a first portion and a second portion, the chamber seal device comprising:

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